EE / CprE / SE 492 – sddec20-proj01
PROJECT TITLE：Machine learning for pilot biometrics
Week 7-8 Report

9/29/2020 – 10/12/2020
Client: Rockwell Collins
Point of contact: JR Spidell
Faculty Advisor: Akhilesh Tyagi

Team members:
Jianhang Liu--Data Manipulation SME
Feng Lin--Hardware SME
Xuewen Jiang --- Camera Interface SME
Xiuyuan Guo --- Algorithm SME
Sicheng Zeng - python SME
Junjie Chen --- C code SME
Sicheng Zeng - Team leader

Bi-weekly Summary

For these two weeks, we continue the work for the last two weeks such as improving the algorithm with various techniques like hyper-parameter tuning, quantization, pruning and hardware acceleration. PCB design hopes it will finish soon, and we will start the PCB layout review this week and hope we can start to order the materials.

Individual Contributions

Xuewen - Finish the bill of materials and get the total price of the daughter card. We are planning to order the board and the parts in several weeks.

Junjie Chen - This week we are working on rebuilding the DPU kernel instead of using the existing ones for maximum flexibility. We are experimenting on different architectures such as ‘leaky relu, average pool’ implementation on the DPU.

Feng Lin-re-compile the face-detection project. Getting familiar with DPU block diagram connectivity and instructions.

Sicheng Zeng- During the last two weeks, I change to a new direction to increase accuracy by using another visualization method. I work on finding which layers and nodes need to remain. I used ANNvisualizer to output a PDF that includes an obvious model tree to show the nodes' relationship. In the next two weeks, I will work on comparing several visualization models.

Xiuyuan Guo- During this time, changed our algorithm by changing the hyperparameter of our model model which include use the early stopping to find the best epoch and the learning rate scheduler to find the best learning rate.

Jianhang Liu- For the last week, Issac and I have finished the raw design of PCB layout of power, camera interface, and ultra96 board interface. In the next 2 weeks, we will continue to work on the layout and improve the traces. We are expected to receive the real PCB board in several weeks.

Team Member	Contribution	Hours Worked for the Week	Total Cumulative Hours
Junjie Chen	Rebuilt the DPU kernel with operation and architecture matching our project	8 h	75 + 8 = 83h
Sicheng Zeng	Use ANNvisualizer to output a model tree and work on increase accuracy	9h	54+10+9= 81h
Xuewen Jiang	Finished BOM and ready to buy the materials	6h	65h
Feng Lin	Re-compile testing project	8h	30 h
Xiuyuan Guo	Change the hyperparameter of the given algorithm and use that to find the best so far to increase the accuracy and decrease latency of algorithm by reduce the layer of the CNN	10h	18+10=28
Jianhang Liu	Following the adjusted schematic, done the Ultra96 board interface part of PCB layout.	6h	65h

Pending Issues

Don’t have experience on assemble PCB and testing
Potential roadblocks on DPU compiling

Plans

1. Optimize total latency about the pruned model running on board.
2. Go through interacting with DPU from python language on an ARM processor .
3. Increase after prune model accuracy